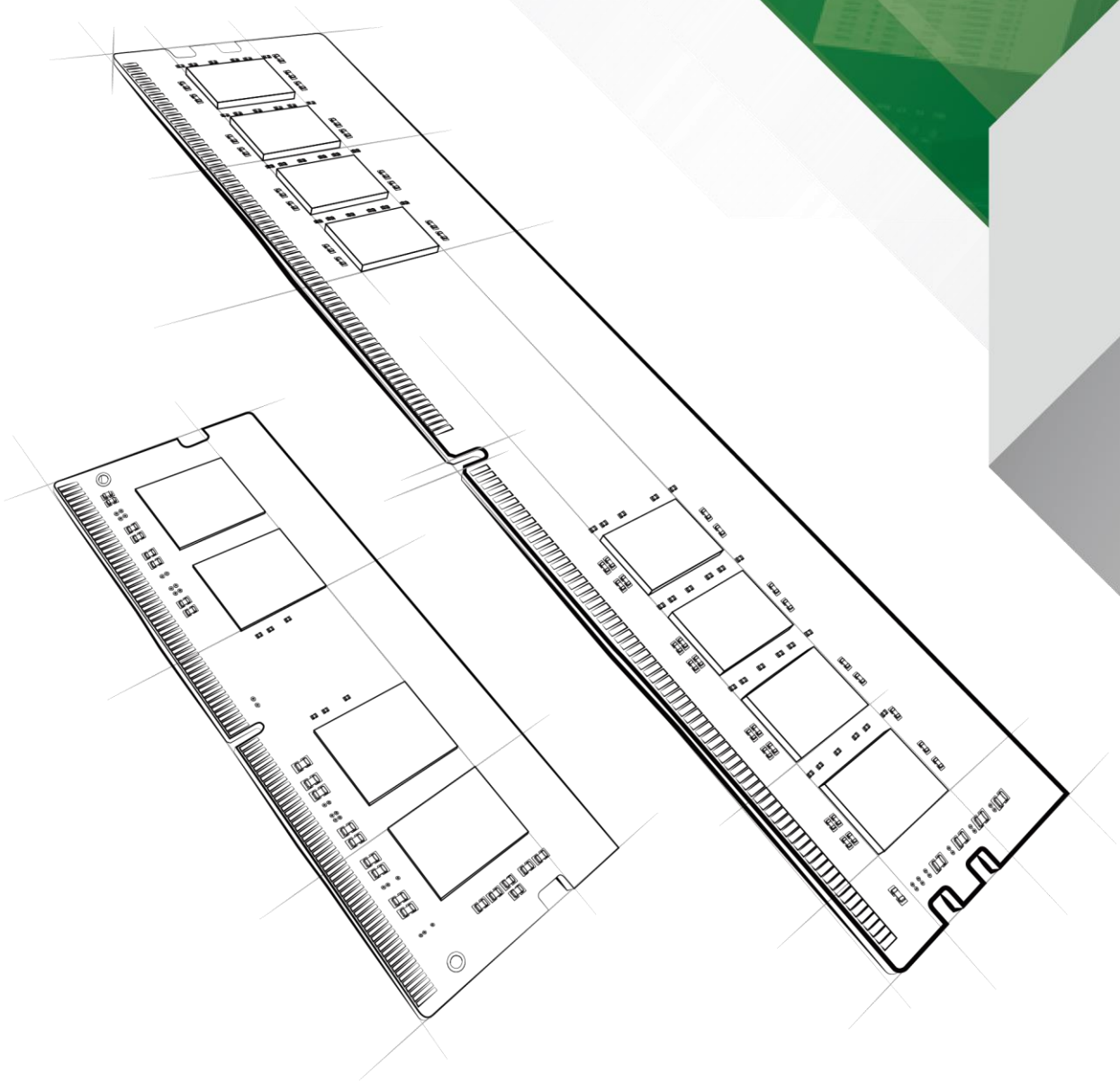
TEAMGROUP Team

INDUSTRIAL



DDR3 SDRAM

U-DIMM Series

Wide Temperature Datasheet

Features

- Fully Tested and Optimized for Stability and Performance
- Uses Original IC to Meet Strict Industrial Standards
- JEDEC Standard 1.35V (1.283V~1.418V) & 1.5V (1.425V~1.575V)
- Operating Environment : -40°C ~ 85°C(TA)
- Lead-free (RoHS compliant)
- CE/FCC Certification
- Gold plating 3u” (30u” for Part Number with –W)

Table of Contents

1. Product Overview

1.1 Introduction

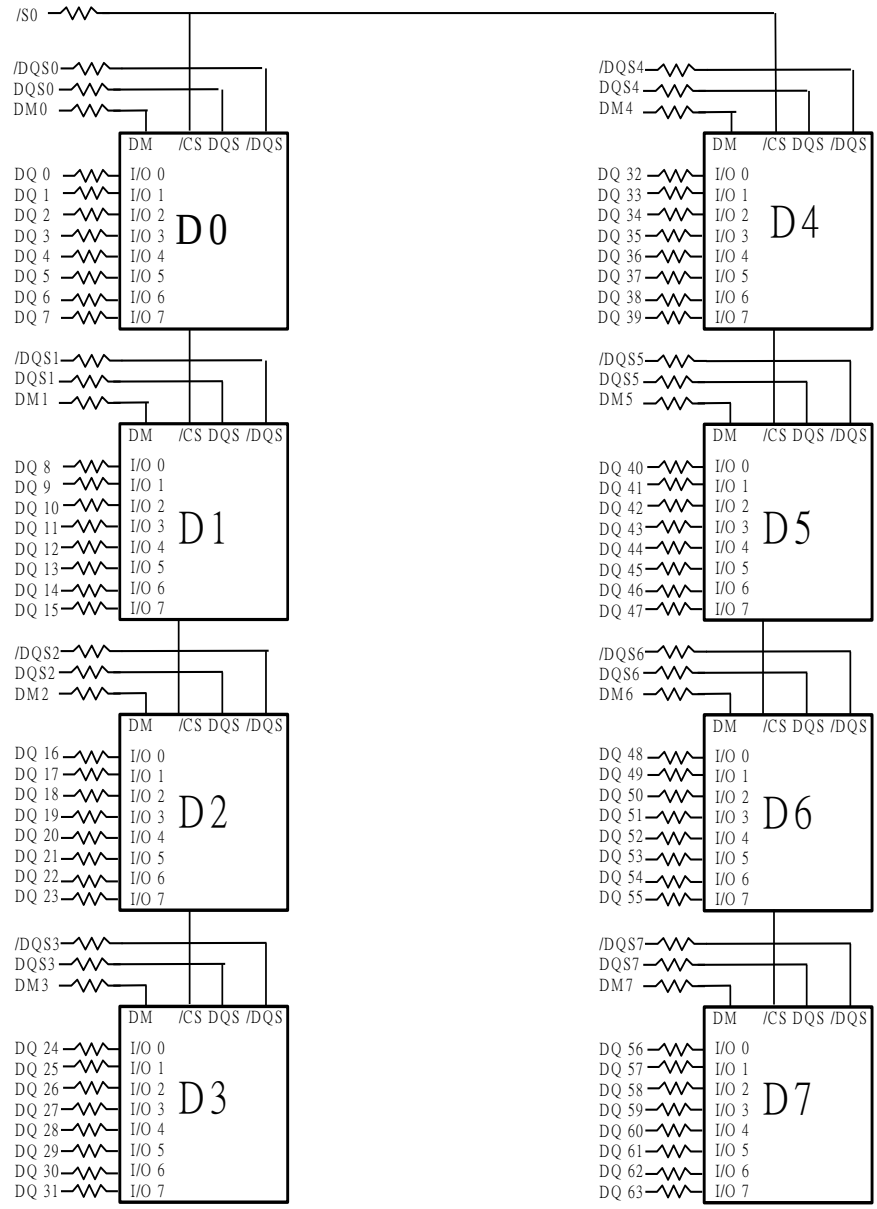
TEAMGROUP announces industrial DDR3 memory module product with leading technology. The products are available in 1.35V~1.5V operating voltage. They have passed strictly controlled processes and are manufactured under rigorous processes. Each memory module has undergone strict testing procedures and burn-in verification, and 100% passed the test. They have high compatibility, stability and excellent performance, which greatly reduces product compatibility issues. They have passed strict electrical interference and noise tests to ensure that no electrical interference will cause problems for each memory module, thus meeting TEAMGROUP Industrial's commitment to meet high-quality requirements. All series of TEAMGROUP memory module products not only use strict production processes to ensure the quality of each memory module, but also provide a lifetime warranty, so you can easily use them and enjoy the best quality.

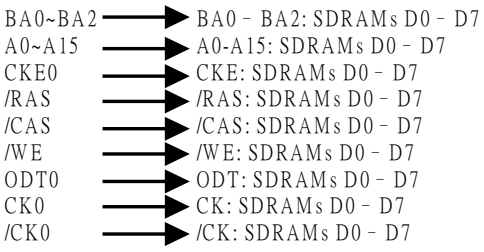
1.2 Interface

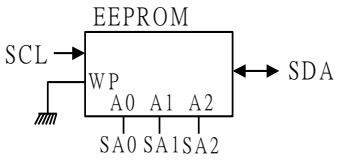
The module is a Dual In-line Memory Module and intended for mounting onto 240-pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

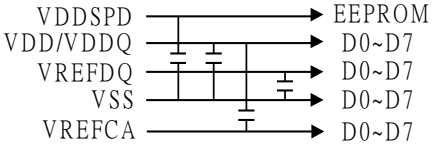
1.3 Block Diagram:

(Populated as 1rank of x8 DDR3 SDRAMs)





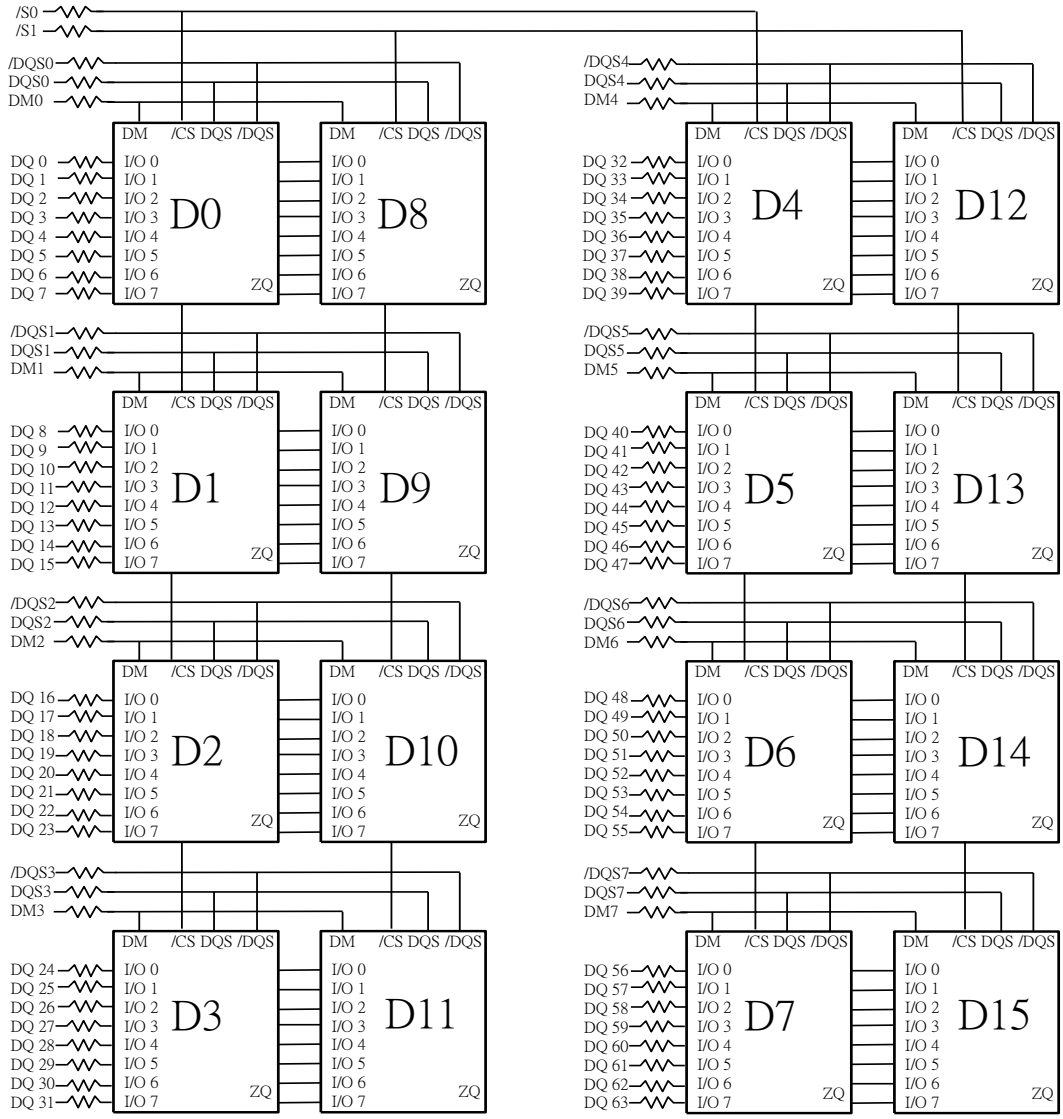


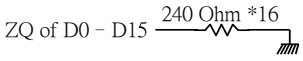


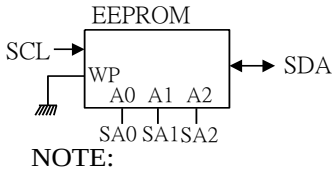
NOTE:

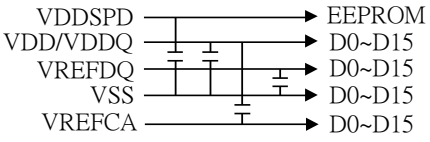
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ,DQS,/DQS,ODT,DM,CKE,/S relationships must be maintained as shown.
3. DQ,DM,DQS,/DQS resistors: Refer to associated topology diagram.

Block Diagram: (Populated as 2rank of x8 DDR4 SDRAMs)









BA0~BA2	BA0 – BA2: SDRAMs D0 – D15
A0~A15	A0-A15: SDRAMs D0 – D15
CKE1	CKE: SDRAMs D8 – D15
CKE0	CKE: SDRAMs D0 – D7
/RAS	/RAS: SDRAMs D0 – D15
/CAS	/CAS: SDRAMs D0 – D15
/WE	/WE: SDRAMs D0 – D15
ODT0	ODT: SDRAMs D0 – D7
ODT1	ODT: SDRAMs D8 – D15
CK0	CK: SDRAMs D0 – D7
/CK0	/CK: SDRAMs D0 – D7
CK1	CK: SDRAMs D8 – D15
/CK1	/CK: SDRA

NOTE:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ,DQS,/DQS,ODT,DM,CKE,/S relationships must be maintained as shown.
3. DQ,DM,DQS,/DQS resistors: Refer to associated topology diagram.
4. For each DRAM,a unique ZQ resistor is connected to ground. The ZQ resistor is 240 Ohm +/-1%

2. Product Specifications

2.1 Device Parameters

MT/s	CL-tRCD-tRP	tCK (ns)	CAS Latency (CLK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)
DDR3-1333	9-9-9	1.5	9	13.5	13.5	36	49.5
DDR3-1600	11-11-11	1.25	11	13.75	13.75	35	48.75
DDR3-1866	13-13-13	1.07	13	13.91	13.91	34	47.91

•JEDEC standard 1.35V(1.283V~1.418V) &

1.5V(1.425V~1.575V) Power Supply

•V_{DDQ} = 1.35V(1.283V~1.418V) & 1.5V(1.425V~1.575V)

•MRS Cycle with address key programs

- CAS Latency (5,6,7,8,9,10,11,13)

- Burst Length (BL):8 and 4 with Burst Chop(BC)

•Bi-directional, differential data strobe (DQS and /DQS)

•DLL aligns DQ and DQS transition with CK transition

•Double-data-rate architecture; two data transfers per clock cycle

•8 independent internal bank

•Internal (self) calibration: Internal self calibration through ZQ pin

•Auto refresh and self refresh

•Average Refresh Period 7.8us

•8-bit pre-fetch.

•On Die Termination using ODT pin.

2.2 CE and FCC Compatibility

Conform to CE and FCC requirements.

2.3 RoHS Compliance

Fully compliant with RoHS directive.

2.4 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	- 0.4 V ~ 1.80 V	V
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	- 0.4 V ~ 1.80 V	V
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	- 0.4 V ~ 1.80 V	V
Storage temperature	T_{STG}	-55 to +100	℃

Note: DDR3 SDRAM component specification

Operating Temperature Condition

Parameter	Symbol	Value	Unit	Note
Operating Temperature Range	TC	-40~+95	℃	1
	TA	-40~+85	℃	2

Note: 1. TC = Case temperature. This is the temperature of the case of the semiconductor device.
2. TA = Ambient temperature. This is the temperature of the environment, still air.

2.5 AC & DC Operating Condition

Parameter	Symbol	Operation	Min	Max	Unit	Note
Supply Voltage	V_{DD}	1. 5	1.425	1.575	V	1,2
	V_{DD}	1.35	1.283	1.418	V	1,2,3
	V_{DDSPD}		3	3.6		
Supply Voltage for Output	V_{DDQ}	1.5	1.425	1.575	V	1,2
		1.35	1.283	1.418	V	1,2,3
I/O Reference Voltage(CMD/ADD)	V_{REF}CA, (DC)		0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	3,4
I/O Reference Voltage(DQ)	V_{REF}DQ, (DC)		0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	3,4
Termination Voltage	V_{TT}		V_{DDQ} /2 - TBD	V_{DDQ} /2 +TBD	V	

Note:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REF} (DC) by more than ±1% V_{DD}. (for reference: approx. ±15mV)
4. For reference: approx. V_{DD} /2 ±15mV.

2.6 Refresh Parameters by Device Density

Parameter	Symbol		512Mb	1Gb	2Gb	4Gb	8Gb	Units
REF command ACT or REF command time	tRFC		90	110	160	260	350	ns
Average periodic refresh interval	tREFI	-40°C≦TA≦85°C	7.8	7.8	7.8	7.8	7.8	us

2.7 Pin Assignment

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
1	$V_{REF}DQ$	121	V_{SS}	60	V_{DD}	180	A3
2	V_{SS}	122	DQ4	61	A2	181	A1
3	DQ0	123	DQ5	62	V_{DD}	182	V_{DD}
4	DQ1	124	V_{SS}	63	CK1,NC	183	V_{DD}
5	V_{SS}	125	DM0	64	/CK1,NC	184	CK0
6	/DQS0	126	NC	65	V_{DD}	185	/CK0
7	DQS0	127	V_{SS}	66	V_{DD}	186	V_{DD}
8	V_{SS}	128	DQ6	67	V_{REFCA}	187	NC,/EVENT
9	DQ2	129	DQ7	68	NC	188	A0
10	DQ3	130	V_{SS}	69	V_{DD}	189	V_{DD}
11	V_{SS}	131	DQ12	70	A10/AP	190	BA1
12	DQ8	132	DQ13	71	BA0	191	V_{DD}
13	DQ9	133	V_{SS}	72	V_{DD}	192	/RAS
14	V_{SS}	134	DM1	73	/WE	193	/S0
15	/DQS1	135	NC	74	/CAS	194	V_{DD}
16	DQS1	136	V_{SS}	75	V_{DD}	195	ODT0
17	V_{SS}	137	DQ14	76	/S1,NC	196	A13
18	DQ10	138	DQ15	77	ODT1,NC	197	V_{DD}
19	DQ11	139	V_{SS}	78	V_{DD}	198	NC
20	V_{SS}	140	DQ20	79	NC	199	V_{SS}
21	DQ16	141	DQ21	80	V_{SS}	200	DQ36
22	DQ17	142	V_{SS}	81	DQ32	201	DQ37
23	V_{SS}	143	DM2	82	DQ33	202	V_{SS}
24	/DQS2	144	NC	83	V_{SS}	203	DM4
25	DQS2	145	V_{SS}	84	/DQS4	204	NC
26	V_{SS}	146	DQ22	85	DQS4	205	V_{SS}
27	DQ18	147	DQ23	86	V_{SS}	206	DQ38
28	DQ19	148	V_{SS}	87	DQ34	207	DQ39
29	V_{SS}	149	DQ28	88	DQ35	208	V_{SS}
30	DQ24	150	DQ29	89	V_{SS}	209	DQ44
31	DQ25	151	V_{SS}	90	DQ40	210	DQ45
32	V_{SS}	152	DM3	91	DQ41	211	V_{SS}
33	/DQS3	153	NC	92	V_{SS}	212	DM5
34	DQS3	154	V_{SS}	93	/DQS5	213	NC
35	V_{SS}	155	DQ30	94	DQS5	214	V_{SS}
36	DQ26	156	DQ31	95	V_{SS}	215	DQ46
37	DQ27	157	V_{SS}	96	DQ42	216	DQ47
38	V_{SS}	158	NC,CB4	97	DQ43	217	V_{SS}

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
39	NC,CB0	159	NC,CB5	98	V_{SS}	218	DQ52
40	NC,CB1	160	V_{SS}	99	DQ48	219	DQ53
41	V_{SS}	161	NC,DM8	100	DQ49	220	V_{SS}
42	NC	162	NC	101	V_{SS}	221	DM6
43	NC	163	V_{SS}	102	/DQS6	222	NC
44	V_{SS}	164	NC,CB6	103	DQS6	223	V_{SS}
45	NC,CB2	165	NC,CB7	104	V_{SS}	224	DQ54
46	NC,CB3	166	V_{SS}	105	DQ50	225	DQ55
47	V_{SS}	167	NC	106	DQ51	226	V_{SS}
48	NC	168	/RESET	107	V_{SS}	227	DQ60
KEY				108	DQ56	228	DQ61
				109	DQ57	229	V_{SS}
49	NC	169	CKE1,NC	110	V_{SS}	230	DM7
50	CKE0	170	V_{DD}	111	/DQS7	231	NC
51	V_{DD}	171	A15	112	DQS7	232	V_{SS}
52	BA2	172	A14	113	V_{SS}	233	DQ62
53	NC	173	VDD	114	DQ58	234	DQ63
54	V_{DD}	174	A12	115	DQ59	235	V_{SS}
55	A11	175	A9	116	V_{SS}	236	V_{DDSPD}
56	A7	176	V_{DD}	117	SA0	237	SA1
57	V_{DD}	177	A8	118	SCL	238	SDA
58	A5	178	A6	119	SA2	239	V_{SS}
59	A4	179	V_{DD}	120	V_{TT}	240	V_{TT}

2.8 Pin Description

Pin Name	Description	Pin Name	Description
A0–A15	SDRAM address bus	SCL	I^2C serial bus clock for EEPROM
BA0–BA2	SDRAM bank select	SDA	I^2C serial bus data line for EEPROM
/RAS	SDRAM row address strobe	SA0–SA2	I^2C slave address select for EEPROM
/CAS	SDRAM column address strobe	V_{DD}	SDRAM core power supply
/WE	SDRAM write enable	V_{DDQ}	SDRAM I/O Driver power supply
/S0–/S1	DIMM Rank Select Lines	$V_{REF}DQ$	SDRAM I/O reference supply
CKE0–CKE1	SDRAM clock enable lines	$V_{REF}CA$	SDRAM command/address reference supply
ODT0–ODT1	On-die termination control lines	V_{SS}	Power supply return (ground)
DQ0–DQ63	DIMM memory data bus	V_{DDSPD}	Serial EEPROM positive power supply
DQS0–DQS8	SDRAM data strobes (positive line of differential pair)	NC	Spare pins (no connect)
/DQS0–/DQS8	SDRAM data strobes (negative line of differential pair)	/RESET	Set DRAMs to Known State
/DM0–DM8	SDRAM data masks/high data strobes	V_{TT}	SDRAM I/O termination supply
CK0–CK1	SDRAM clocks (positive line of differential pair)		
/CK0–/CK1	SDRAM clocks (negative line of differential pair)		

2.9 Power Consumption

Symbol	Description
IDD0	Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /S is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD1	Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W
IDD2P	Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING
IDD2Q	Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /S is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING
IDD2N	Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /S is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD3P	Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING
IDD3N	Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD4R	Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W
IDD4W	Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /S is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R
IDD5B	Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /S is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD6	Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING
IDD7	Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, /S is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R

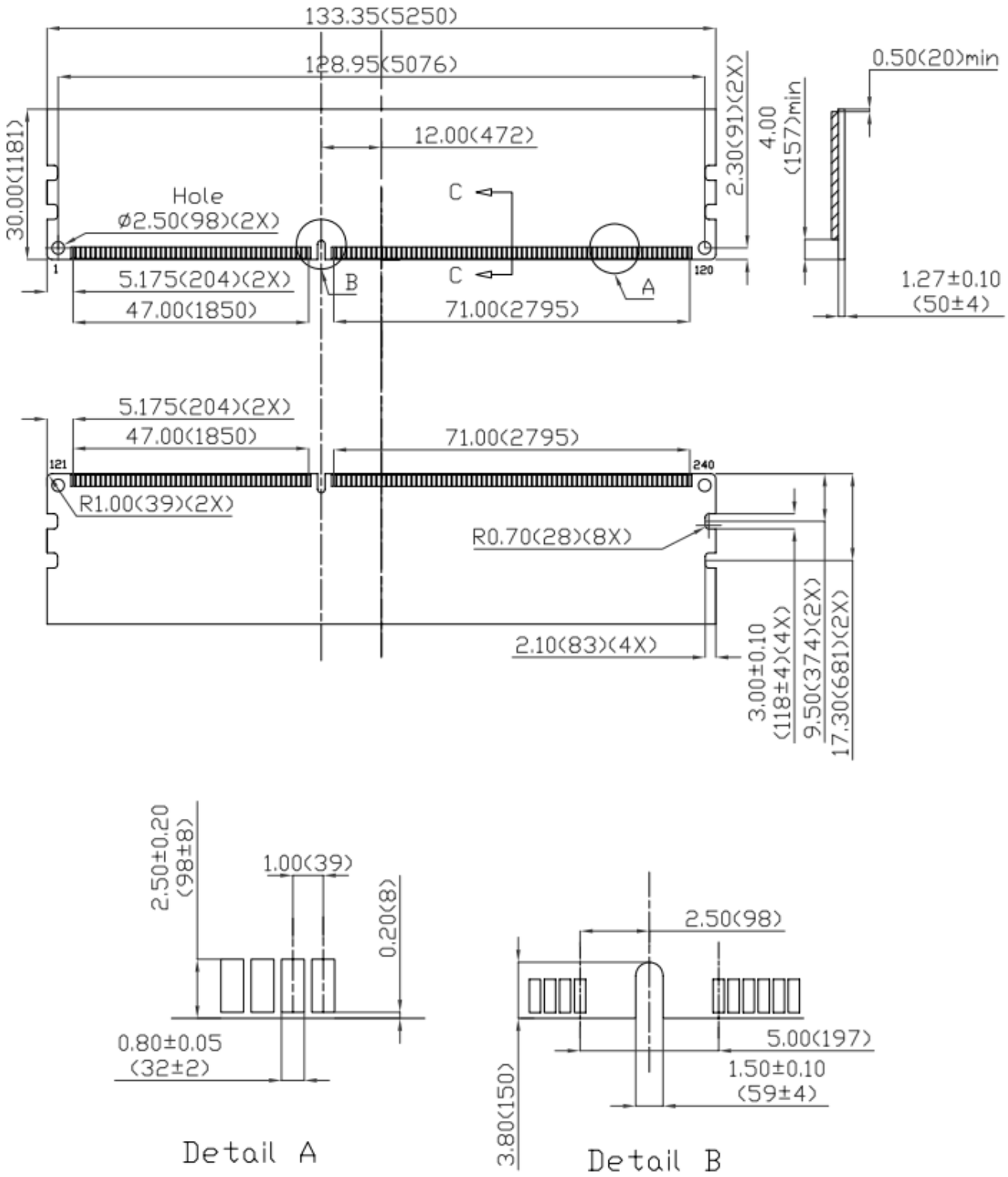
1RANK

Symbol	DDR3 1333 9-9-9		DDR3 1600 11-11-11		DDR3 1866 13-13-13		Unit
	1.5V	1.35V	1.5V	1.35V	1.5V	1.35V	
IDD0	240	208	252	225	264	242	mA
IDD1	304	272	312	286	328	304	mA
IDD2P	88	64	92	72	96	85	mA
IDD2Q	128	96	136	110	152	136	mA
IDD2N	136	104	144	118	160	142	mA
IDD3P	120	88	125	92	128	98	mA
IDD3N	168	136	176	146	192	160	mA
IDD4R	600	520	640	560	680	620	mA
IDD4W	640	560	680	600	735	650	mA
IDD5B	1120	1000	1170	1050	1225	1112	mA
IDD6	104	80	108	84	112	91	mA
IDD7	1040	920	1080	960	1160	1000	mA

2RANK

Symbol	DDR3 1333 9-9-9		DDR3 1600 11-11-11		DDR3 1866 13-13-13		Unit
	1.5V	1.35V	1.5V	1.35V	1.5V	1.35V	
IDD0	376	312	416	344	513	486	mA
IDD1	440	376	480	408	525	544	mA
IDD2P	176	128	196	148	216	176	mA
IDD2Q	256	202	272	222	310	262	mA
IDD2N	272	208	288	232	322	288	mA
IDD3P	240	176	262	200	288	232	mA
IDD3N	336	272	352	298	383	320	mA
IDD4R	736	624	816	696	875	740	mA
IDD4W	760	692	820	736	900	800	mA
IDD5B	1256	1104	1296	1136	1376	1200	mA
IDD6	208	160	216	180	234	208	mA
IDD7	1176	1024	1256	1096	1321	1240	mA

2.10 Physical Dimensions



Detail A

Detail B

Note：All dimensions are in millimeters(mils) and should be kept within a tolerance of ±0.15,unless otherwise specified.

3. Ordering Information

Speed	Capacity	Part Number
1333	4GB	TE4GKLXW3HS-W
1333	8GB	TE8GKLXW3HS-W
1600	4GB	TE4GKLXW6HS-W
1600	8GB	TE8GKLXW6HS-W
1866	4GB	TE4GKLXW8HS-W
1866	8GB	TE8GKLXW8HS-W

Speed	Capacity	Part Number
1333	4GB	TE4GKLXW3HH-V
1333	8GB	TE8GKLXW3HH-V
1600	4GB	TE4GKLXW6HH-V
1600	8GB	TE8GKLXW6HH-V
1866	4GB	TE4GKLXW8HH-V
1866	8GB	TE8GKLXW8HH-V

4. Part Number Rule

1	2	3	4	5	6	7	8	9		10
TE	4G	K	L	X	W	6	H	S	-	W

1. TE
- TeamGroup Embedded

2. Capacity:
- 2G : 2GB
- 4G : 4GB
- 8G : 8GB

3. Generation:
- K : DDR3

4. Form Factor:
- S : SO-DIMM
- L : Long-DIMM
- R : R-DIMM

5. Memory Bus Width
- X : 64
- E : 72

6. Voltage
- V : Standard Voltage(1.5V)
- W : Low Voltage(1.35V)

7. Speed
- 1：1066
- 3：1333
- 6：1600
- 8：1866

8. DRAM Config
- U：128Mx8
- N：256Mx8
- H：512Mx8

9. Brand
- S：Samsung
- M：Micron
- H：Hynix

10.Operating Temp
- V : Value-added Temp[1]
- W : Wide Temp[2]

Note :

1. Using original DRAM IC with wide temperature sorting technology
2. Using original wide temperature (industrial grade) DRAM IC

5. Revision History

Version	Description	Date	NOTES
1.0	Initial Release	10-July-2019	
2.0	Ordering Information	22-April-2020	
2.1	Updated Part Number Rule	22-June-2020	

Global Presence

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